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Technical Memorandum

SSMIR - A NEW APPROACH TO ACQUIRING DATA DURING AN AIRCRAFT SEAT/SLED EJECTION SEQUENCE

by

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15 April 1985

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NAVAL AIR TEST CENTER
PATUXENT RIVER, MARYLAND

DEPARTMENT OF THE NAVY
NAVAL AIR TEST CENTER
PATUXENT RIVER, MARYLAND 20670-5304

TM 85-3 SY
15 April 1985

Anthropomorphic manikins currently used for aircraf' ejection seat testing are equipped with a telemetry/pulse code modulation (T. I/PCM) system. During ejection seat sled testing, telemetered data have been lost, negating very expensive test programs. A Solid State Memory Instrumentation Recorder (SSMIR) was developed jointly by NAVAIRTESTCEN (Advanced Technology funds) and NAVAIRDEVCEN (N62269/83/WR/00421) to parallel the TM/PCM. The SSMIR was developed as a nonvolatile recording device to back up the TM/PCM system and thus avoid possible loss of data. This technical memorandum describes in detail the development, test, and evaluation of the SSMIR.

APPROVED FOR RELEASE:

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O. D. TIMM, Acting
Commander, Naval Air Test Center

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER TM 85-3 SY	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) SSMIR - A NEW APPROACH TO ACQUIRING DATA DURING AN AIRCRAFT SEAT/SLED EJECTION SEQUENCE		5. TYPE OF REPORT & PERIOD COVERED TECHNICAL MEMORANDUM 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) DANIEL M. WATTERS RICHARD P. WHITE, JR. RONALD J. SPICUZZA		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS NAVAL AIR TEST CENTER SYSTEMS ENGINEERING TEST DIRECTORATE PATUXENT RIVER, MARYLAND 20670-5304		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS NAVAL AIR TEST CENTER NAVAL AIR STATION PATUXENT RIVER, MARYLAND 20670-5304		12. REPORT DATE 15 APRIL 1985 13. NUMBER OF PAGES 19
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

(cont hpc)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

SOLID STATE INSTRUMENTATION RECORDER
NONVOLATILE MAGNETIC BUBBLE MEMORY;
ANTHROPOMORPHIC DUMMIES;
SLED EJECTION SEAT TESTING.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The current state of ejection seat/sled testing employs an Aydin/Vector Company Pulse Code Modulation/Telemetry (PCM/TM) instrumentation package. While this system meets all channel/data rate requirements and has proven itself in field testing over the years, some major deficiencies exist. Data turnaround is one drawback; up to several weeks are normally required to process and print out the results from any sled shot. The resulting delay is not acceptable in the current era of high-speed computer technology. A second major deficiency is the amount of lost data (data dropout) that can occur. In an ejection seat test, orientation of the skull antenna or misalignment of sending and receiving

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antennas can result in loss of data. Current technology in data storage media and high-speed controllers provides backup mode for data integrity and also permits faster data reduction. This paper presents a summary of an electrical/mechanical packaging design of a software controlled, nonvolatile data recording system which utilizes 8 megabits of bubble memory to provide 24 sec of data storage in parallel to the PCM/TM transmission. Preliminary laboratory bench testing of the Solid State Memory Instrumentation Recorder indicates that the bubble memory can withstand the high vibration g loads (20 Gs up to 2000 Hz) and environmental temperatures (85°C) encountered in ejection seat testing. Laboratory shock testing (ejection seat trainer) to 5 Gs has also been successful along with tower testing at the Naval Air Development Center to 25 Gs.

SUMMARY

The current state of ejection seat/sled testing employs an Aydin/Vector Company Pulse Code Modulation/Telemetry (PCM/TM) instrumentation package. While this system meets all channel/data rate requirements and has proven itself in field testing over the years, some major deficiencies exist. Data turnaround is one drawback; up to several weeks are normally required to process and print out the results from any sled shot. The resulting delay is not acceptable in the current era of high-speed computer technology. A second major deficiency is the amount of lost data (data dropout) that can occur. In an ejection seat test, orientation of the skull antenna or misalignment of sending and receiving antennas can result in loss of data. Current technology in data storage media and high-speed controllers provides backup mode for data integrity and also permits faster data reduction. This paper presents a summary of an electrical/mechanical packaging design of a software controlled, nonvolatile data recording system which utilizes 8 megabits of bubble memory to provide 24 sec of data storage in parallel to the PCM/TM transmission. Preliminary laboratory bench testing of the Solid State Memory Instrumentation Recorder indicates that the bubble memory can withstand the high vibration g loads (20 Gs up to 2000 Hz) and environmental temperatures (85°C) encountered in ejection seat testing. Laboratory shock testing (ejection seat trainer) to 5 Gs has also been successful along with tower testing at the Naval Air Development Center to 25 Gs.

(SSMI)

Keywords: (To 1473)

SSMIR - A NEW APPROACH TO ACQUIRING DATA DURING AN AIRCRAFT SEAT/SLED EJECTION SEQUENCE

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ABSTRACT. The current state of ejection seat/sled testing employs an Aydin/Vector Company Pulse Code Modulation/Telemetry (PCM/TM) instrumentation package. While this system meets all channel/data rate requirements and has proven itself in field testing over the years, some major deficiencies exist. Data turnaround is one drawback; up to several weeks are normally required to process and print out the results from any sled shot. The resulting delay is not acceptable in the current era of high speed computer technology. A second major deficiency is the amount of lost data (data dropout) that can occur. In an ejection seat test, orientation of the skull antenna or misalignment of sending and receiving antennas can be disastrous. Current technology in data storage media and high speed controllers provides an alternate back-up mode for data integrity and also permits faster data reduction. This paper presents a summary of an electrical/mechanical packaging design of a software controlled, nonvolatile data recording system which utilizes 8 megabits of bubble memory to provide 24 seconds of data recording and storage in parallel to the PCM/TM transmission.

Preliminary bench testing of the Solid State Memory Instrumentation Recorder (SSMIR) indicates that the bubble memory can withstand the high G loads (20 Gs up to 200 Hz) and environmental temperatures (85°C) encountered in ejection seat testing. Laboratory shock testing to 5 Gs has also been successful along with tower testing at the Naval Air Development Center (NADC) to 25 Gs.

INTRODUCTION. In order to evaluate various means of protecting a pilot from serious injury during ejection from high speed aircraft, instrumented anthropomorphic manikins are ejected from aircraft cockpits traveling at high speeds on sled tracks. The PCM/TM instrumentation embedded within the test manikins receives the signals from the various transducers and conditions the signals which are then telemetered to the ground station. While this procedure has been used for many years, it has not necessarily proven to be a reliable means of obtaining data. One of the main problems associated with telemetering data from a free flight of a manikin during ejection is the loss of the telemetered signals if the manikin/seat combination is unstable, and the antenna is masked from the ground station. Triangularization of ground station receivers, while improving the probability of receiving the transmitted data from a manikin in unstable flight, has not resolved the problem. Since the cost expenditure for a sled ejection test is relatively large, efforts are being directed toward developing on-board memory systems to record the data that in the past has been telemetered. For example, the Navy has developed a Block Organized Random Access Memory/Metal Nitride Oxide Semiconductor (BORAM/MNOS) nonvolatile memory system for storing data prior and during an aircraft incident or crash. The BORAM/MNOS system has proven to be a highly reliable recording system in a very adverse environment. While the direct application of the BORAM/MNOS unit to anthropomorphic test manikins would seem to be desirable, its capacity for write speed and magnitude of data acquisition is not sufficient for this type of dynamic testing.

Advanced nonvolatile magnetic bubble memory units have been developed for many applications associated with severe environments and remote locations. Because of the advances made in recent years in the development of bubble memory systems, their small size and large capacity makes them a prime candidate for use in anthropomorphic test manikins. The purpose of the effort reported in this paper was to develop a SSMIR using existing and available bubble memory devices and to integrate the SSMIR in an existing anthropomorphic instrumentation system and through test to evaluate their applicability to the ejection test environment.

TECHNICAL DISCUSSION. The experimental application of bubble memory devices to anthropomorphic test manikins for evaluation had to consider a number of factors to ensure that the evaluation was conducted successfully and properly. In addition to developing a proper interface buffer unit between the existing Vector PCM/TM and the bubble memory devices, modifications to the power and battery storage units had to be considered as well as the proper packaging of the complete PCM/TM instrumentation system within the cavity of the anthropomorphic manikin. A brief summary of the considerations that were given to the

development of the SSMIR system will be presented in this section of the paper.

The basic assumptions made in the SSMIR development were as follows:

1. The existing Vector PCM/TM unit would be utilized for sensor data acquisition and conditioning.

2. Modification of the smart memory buffer unit developed by SRL for the Limb Restraint Evaluator (LRE) would be undertaken to provide the proper control interface between the Vector PCM/TM and the SSMIR.

3. Intel bubble memory devices that were immediately available would be used as the nonvolatile memory.

4. The SSMIR package would be designed to fit both the 3rd percentile and the 98th percentile manikins.

5. A 95th percentile center-of-gravity (CG) manikin with the associated Vector PCM/TM instrumentation system would be used as the basic test system to which the SSMIR would be integrated.

As previously noted, it was desired to add a bubble memory system to the standard CG manikin instrumentation so that the data could be telemetered, as well as recorded by the SSMIR. This approach required that the SSMIR work in parallel with the standard telemetering instrumentation. Figure 1 presents a block diagram of the SSMIR/PCM/TM system. As can be seen, the existing PCM/TM sends its data to the transmitter and antenna and the same signals are fed to the SSMIR bubble memory system.

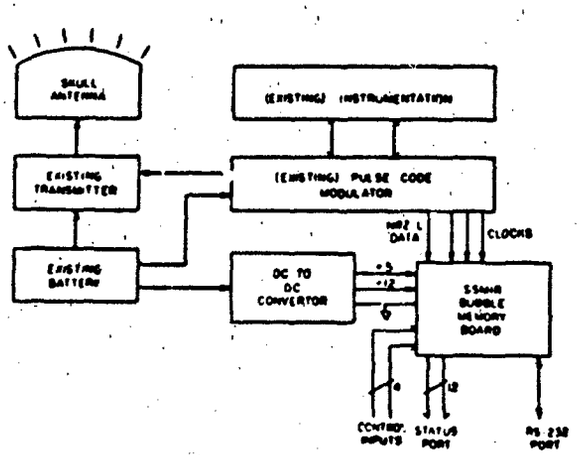

Figure 1. SSMIR System Block Diagram

The Vector PCM/TM system that was integrated with the SSMIR was the Vector ADS-100 Series which is a completely self-contained data acquisition, conditioning, and transmission system. The latest configuration has 32 high level multiplexed channels, as well as 16 low level multiplexed channels, and 24 bi-level multiplexed channels. This is accomplished via the 600 Series PCM/TM Multiplexer/Encoder which is versatile and compact. It is extremely flexible because of the Electrically Programmable Read Only Memory (EPROM) controlled configuration which allows changes in the system to occur with few, if any, hardware changes. The battery pack associated with the PCM/TM provides +28 VDC and 2.2 amp hours. It weighs 6 3/8 pounds and occupies a volume of 100 cubic inches. As indicated in Figure 1, the existing battery pack in the Vector PCM/TM was also used to power the SSMIR.

BUBBLE MEMORY DEVICE. The magnetic bubble memory devices used are manufactured by Intel. Both the 4 megabit and 1 megabit memory devices were investigated for use in the SSMIR.

The pertinent data regarding the Intel devices are as follows:

- 1 Megabit Device
  - Operating Frequency, 50 KHz
  - Field Rotation Frequency, 50 KHz
  - Maximum Data Rate, 100 K Bits/Second
- 4 Megabit Device
  - Operating Frequency, 100 KHz
  - Field Rotating Frequency, 100 KHz
  - Maximum Data Rate, 400 K Bits/Second

Based on information obtained from Intel, samples of the 4 megabit bubble devices would probably not be available until near the end of the first quarter of 1984, and preproduction units would not be available until some time in the second half of 1984. Because of the late availability of the 4 megabit devices, the 1 megabit devices were used in the SSMIR design.

Since the bubble devices access requires 160 milliseconds of setup time and 4 millisecond interpage pause delay time between page writes and variable seek page delays, a simple design could not be used to store time varying data on a continuous basis. In addition, the slower write speed of the bubbles would not allow the data output from the Vector PCM/TM to be written in real-time. Because of these two noted characteristics of the bubble memory system, an intermediate buffer memory system

was required. This buffer memory system must also be microprocessor controlled since the bubble memory has pause times in its writing capability. A slight modification of the smart memory buffer system developed by SRL for the LRE was used to provide this interface between the Vector PCM/TM and the bubble memory devices. Also, with the maximum bubble data rate of 100 K bits/second and the PCM/TM fixed data rate of 300 K bits/second, the firmware for the system was written to separate four bubble memories in parallel to get an effective maximum data rate of 400 K bits/second. (This rate does not include access delay.) This parallel operation allows the actual PCM/TM data rate and bubble data rate to be closer matched in actual speed and, as a result, allows the intermediate buffer memory to be reduced to 2 K static RAM memory words for buffering of the incoming PCM/TM data. This buffering in a FIFO (first in-first out) fashion takes up the slack in speed differences that are continually varying during the bubble writing process.

NONVOLATILE SSMIR SYSTEM. Figure 2 presents a block diagram of the SRL smart memory buffer unit and the bubble memory system. The system captures serial PCM/TM data and saves it in the nonvolatile bubble memory subsystem for posttest retrieval and analysis. As previously noted, the slow access times of the nonvolatile bubble memory requires the buffering of the incoming "real-time" PCM/TM data in a 2 K word Static Random Access Memory (SRAM) Array. The system is software driven by a Motorola MC68000 Central Processing Unit, executing a firmware program stored in nonvolatile EPROM. Data are later removed from the bubble memories using an RS-232C asynchronous serial data port.

68000 CPU AND CLOCK. The Central Processing Unit (CPU), the heart of the system, directly or indirectly controls all data manipulations, timing, control operations, and line transfers to all other elements of the system. The central clock drives the CPU, which in turn drives everything else. Also associated with the logic is the power-on reset circuitry which initializes the system following application of power.

PCM DECODER. The Pulse Code Modulator (PCM) decoder converts the incoming NRZ-L serial data stream (from the data diagnostic output of the PCM) into a 16 bit "word" for saving in the system memory systems. Once the "start-capture" signal is received, the next PCM generated "frame" clock enables the PCM

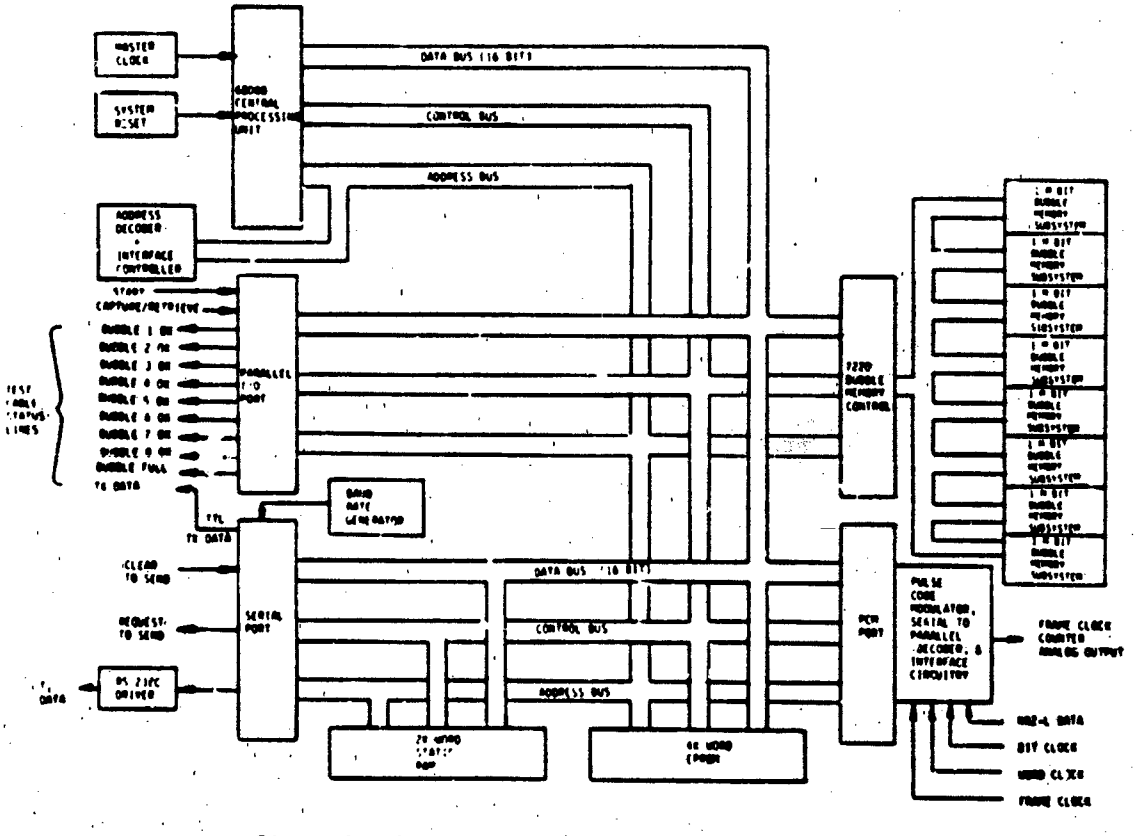

Figure 2. Computer System-Magnetic Bubble Memory

decoder. Two 8 bit "words" are serially shifted in, using the PCM "bit" clock and latched, for transfer by the CPU to the SRAM array. Another circuit in the section increments an 8 bit counter every time a "frame" clock is received. The counter drives an 8 bit (voltage) Digital-to-Analog Converter (D/AC) which, in turn, drives a high level analog input to the PCM. This "frame counter" enables easier and accurate alignment of data from the bubble memory with data from the telemetry system for posttest data analysis.

EPROM. The nonvolatile EPROM program storage memory (4 K words) contains three major routines. The first routine is the initialization routine which is run at power-application time to condition the I/O ports and test system operational capabilities via diagnostic routines. The second routine is the data "capture" routine, which is run when mode control switching indicates "start-capture." The data is taken from the PCM interface port and saved in the SRAM buffer memory at a real-time data rate. The data are moved from the SRAM Array to the bubble memory when the bubble memory is able to receive it. Data "capture" ceases when 8 megabits of data have been stored. The third routine is the data "retrieval" routine, which is run when mode control switches indicate "start-retrieval." Once data have been placed in the magnetic bubble memory, it must be extracted in some orderly, logical manner. This data extraction is performed by serial data transfers and to do serial transfers, it is necessary to have an 8 bit Universal Asynchronous Receiver Transmitter (UART) which is configured to transmit data in a RS-232C serial link. The data retrieval is a nondestructive read operation; the data remains in the bubble memory until it is purged or written over.

PACKAGING OF INSTRUMENTATION SYSTEM. Figure 3 is a photograph of a 95th percentile CG manikin with the Vector PCM/TM installed in the chest cavity. This picture shows there is little or no room for additional instrumentation within the chest cavity. Because of the limited space, an approach had to be considered to include the SSMIR data recording system within the confines of the dummy as shown in Figure 4. The existing door of the dummy was replaced with a new door which slightly altered the body contour. The DC/DC voltage converters were placed in the neck region of the manikin.

A desirable design feature of this packaging scheme was that it could be utilized with both the 3rd percentile and 98th percentile manikins. The primary difference between the 3rd and 98th percentile manikin is that the curved sides of the 98th percentile manikin, are straight in the 3rd percentile manikin, and the door of the 3rd percentile manikin is flat. The remaining challenge was to incorporate the entire SSMIR instrumentation package within the modified door. The manner which this was accomplished is shown in Figure 5. A high density, two-sided PC board was used with the support electronics on the back side of the board under each bubble memory device. Figure 6 shows a photograph of the SSMIR system mounted on the board and incorporated within the door. In this photograph, the 68000 CPU and its associated electronics are covered with a protective shield. Figure 7 shows the SSMIR system with the interconnect wiring to the PCM/TM and the DC/DC power converter prior to attaching the door to the manikin. Figure 8 shows the SSMIR system attached to the manikin. As can be seen, the SSMIR door does not protrude outside of the flesh covering around the thorax; and when the flight suit and seat harness are put in place, there is no noticeable change in the body contour or in the manner in which the harness interacts with the body (Figure 9). Another advantage of having the entire SSMIR system in the door of the manikin is that after a test, the entire data package can be quickly removed and taken into a data reduction and analysis laboratory.

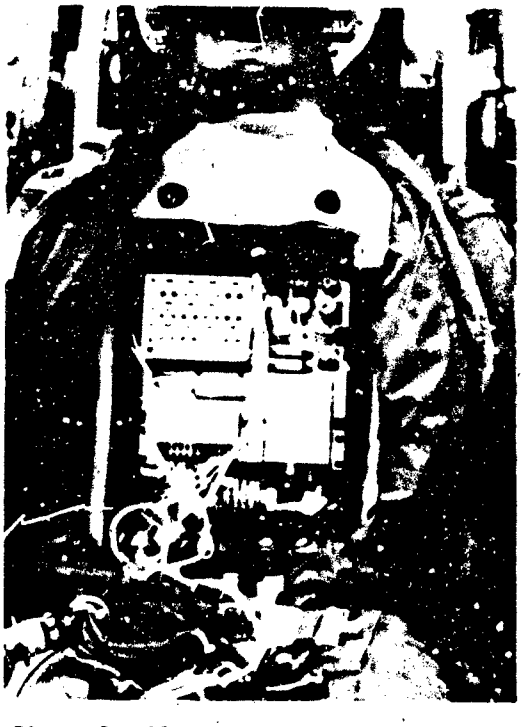

Figure 3. 95th Percentile CG Manikin with Vector PCM/TM

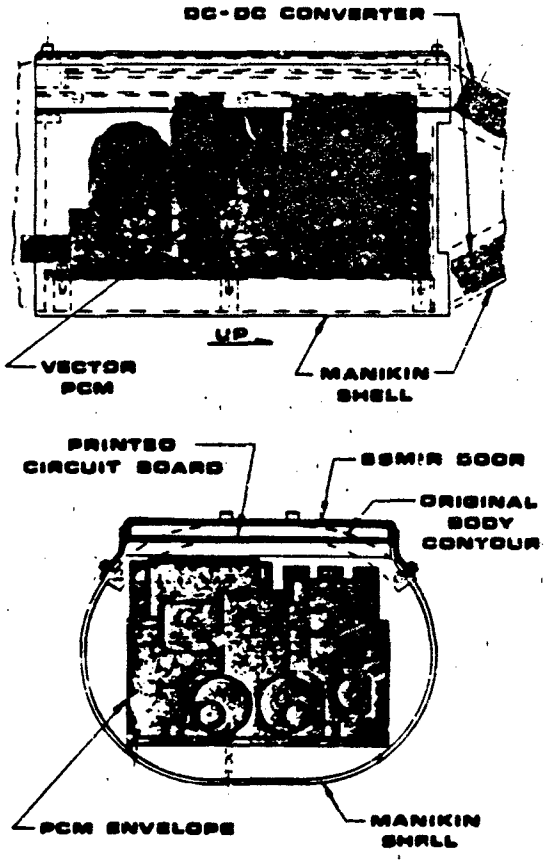

Figure 4. Mechanical Assembly and Installation

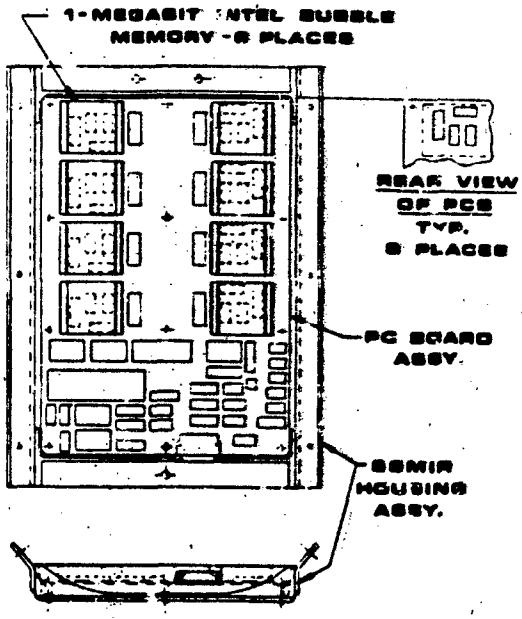

Figure 5. Bubble Memory PCB Assembly and Installation

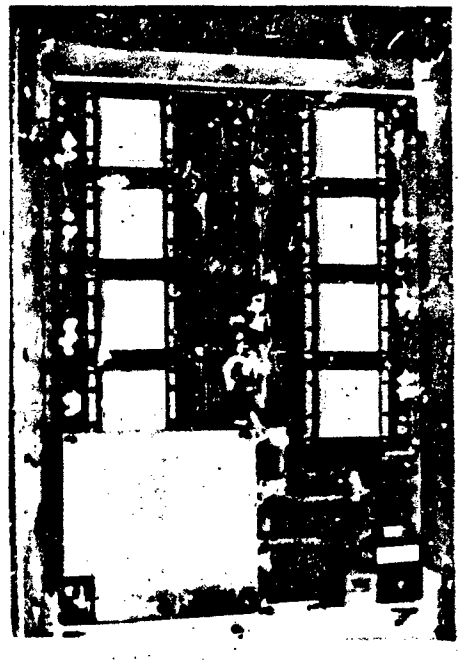

Figure 6. SSMIR System in Manikin Door

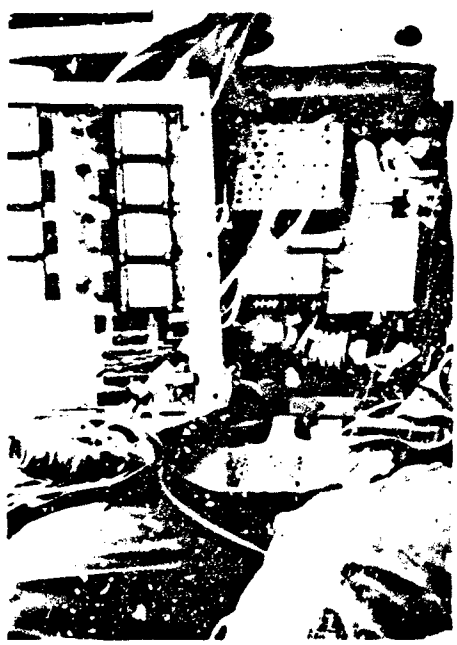

Figure 7. SSMIR/PCM/TM System

Figure 8. SSMIR Attached to 95th Percentile Manikin

Figure 9. SSMIR Test Manikin Ready for Test

SYSTEM CHECKOUT TESTING. Both laboratory and ejection tower testing have been undertaken to verify the operation of the SSMIR system in the operational environment. Each of the major areas of testing are discussed separately.

LABORATORY TESTING. A number of environmental compatibility tests were conducted with various critical system components to investigate their compatibility with the anticipated operational environment. An area of major concern was the ability of the PCM/TM battery to power both the PCM/TM and the SSMIR system through the DC/DC converter which supplied ±5 and ±12 VDC to the SSMIR. In order to evaluate the capabilities of the PCM/TM battery to power both systems under the various environmental temperature conditions, the PCM/TM battery pack was tested in the SRL temperature chamber. The battery was fully charged and power loaded with dummy power load. The battery voltage was then monitored as a function of time. Figure 10 presents the results of these tests. It is apparent that the battery is more than satisfactory for the time period the system would be under full power (<5 minutes). The efficiency of the DC/DC converter over the range of voltages anticipated is presented in Table 1. The Intel magnetic bubble devices were also subjected to the same temperature tests. Figure 11 shows a bubble memory device in the environmental chamber

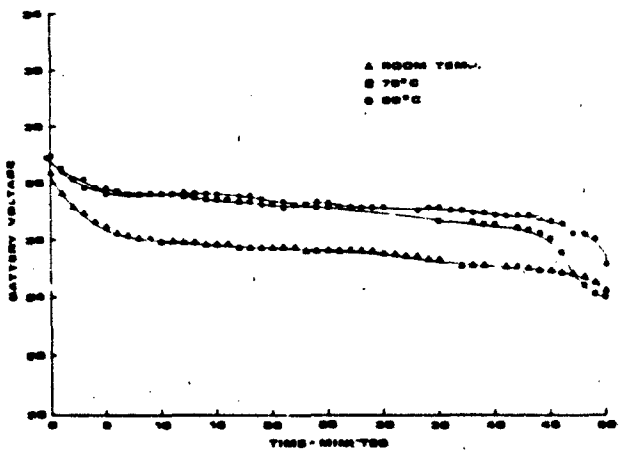

Figure 10. PCM/TM Battery Voltage as a Function of Time

TABLE 1. SSMIR DC-DC CONVERTER LOAD TESTS

Input Volts	Input Amps	Input Watts	5 V Out Amps	12 V Out Amps	Out Watts	Efficiency (percent)
			2/3 Load			
23.0	3.02	69.46	2.0	2.666	42	60.47
24.0	3.02	72.48	2.0	2.666	42	57.95
25.0	3.02	75.50	2.0	2.666	42	55.63
26.0	3.05	79.30	2.0	2.666	42	52.96
27.0	3.08	83.16	2.0	2.566	42	50.50
28.1	3.08	86.55	2.0	2.666	42	48.53
			Full Load			
23.0	4.45	102.35	3.0	4.000	63	61.55
24.0	4.45	106.80	3.0	4.000	63	58.99
25.0	4.45	111.25	3.0	4.000	63	56.63
26.0	4.45	115.70	3.0	4.000	63	54.45
27.0	4.50	121.50	3.0	4.000	63	51.85
28.1	4.53	126.84	3.0	4.000	63	49.67

Figure 11. Bubble Memory Unit in Test Chamber

along with its supporting electronics. Figure 12 is a photograph of the bubble system controller/evaluation/diagnostic PC board. By using this test system, the operation of the bubble memory system could be exercised and system failures recorded. The tests were conducted by first evaluating the system operation at room temperature in the test chamber. The chamber was then brought to 65°C and stabilized over a 2-hour period and its operation checked over a 1/2 hour time interval. The temperature was then raised 5°C over a half hour time period and the system operated and checked over a 1/2 hour time interval. This same procedure was repeated through 85°C for all of the eight bubble devices. Although the Intel bubble devices (Model 7110-1) were only guaranteed for proper operation up to 75°C, they all operated properly up to 85°C.

Figure 12. Bubble System Controller/ Diagnostic Unit

Using the same bubble control system used for the temperature tests, each of the bubble devices and their supporting electronics were tested over the frequency range of 10 to 2000 Hz at a constant oscillating amplitude of 20 Gs along all of their principle axes. All bubble units satisfactorily passed these tests.

The operation of the entire SSMIR system was checked out in the laboratory using an HP 64000 Computer Development System. The HP 64000 Computer Development System was also used to develop and test the SSMIR system control firmware. To perform these tests, a PCM simulator was developed to duplicate the operation of the Vector PCM system. It was believed that, during the checkout of the SSMIR system, this was a much more efficient procedure than using the Vector PCM system because of the limited operating time on the batteries. During the checkout of the SSMIR, it was determined that the bubble memory units

would not operate properly when the 5 V supply dropped below 4.95 V. Intel states the bubble system should operate properly if the 5 V was as low as 4.68 V. The reason for this difference in the limits on the 5 V supply for the proper operation of the bubble memory unit was never resolved. A similar sensitivity of the 12 V system was not noted in check-out and testing.

It was also noticed that power transients during power-up in the 5 V power supply could cause the bubble memory system to lose its control "boot" which designates which of the bubbles in each memory unit are activated. To correct this problem, the "boot" mask was placed in the EPROM and the "boot" mask is down loaded into the bubble memories on every system power-up. The final set of laboratory tests were conducted with the complete system incorporated in the 95th percentile dummy. These tests were conducted in the Ejection Sequence Trainer at the Naval Air Test Center (NATC) at Putuxent River, Maryland. Tests up to 5 Gs indicated that the system operated properly as all acceleration data were recorded and later recovered from the bubble memory devices.

FIELD TESTING. Proof of concept testing was conducted with the SSMIR system on the ejection tower at the Naval Air Development Center (NADC), Warminister, Pennsylvania, in August 1984. Test shots were conducted at nominal G values of 12, 18, and 24 Gs. Figure 13 shows a photograph of an engineer conducting a bubble system check just prior to the test. The power umbilical running up from the lower left of the picture is disconnected once the PCM/TM gyros are brought up to speed. The trigger for the start of the data collection was a pull-out wire attached to a fixed structure which opened up a circuit as the seat started up the rails. Figure 14 shows the manikin on the tower at the completion of the ejection sequence, and Figure 15 shows how the data were off-loaded from the SSMIR for analysis approximately 5 minutes after the ejection sequence was completed.

Figure 16 presents a summary plot of the Gz data obtained during the tests in the ejection tower. Results are presented for the nominal 12 G shot and the 25 G shot (the 18 G data were inadvertently erased). It is noticed from the plot that approximately 1 1/2 to 2 Gs were applied to the dummy before data were recorded by the SSMIR system. This delay in recording was due to the time required to pull the "start" wire out of its connection during the initial travel of the seat. In both the nominal 12 G and 24 G shot, there was a rapid build up of the acceleration, then a decrease followed by a build up to the maximum G

Figure 13. System Check Just Prior to Test

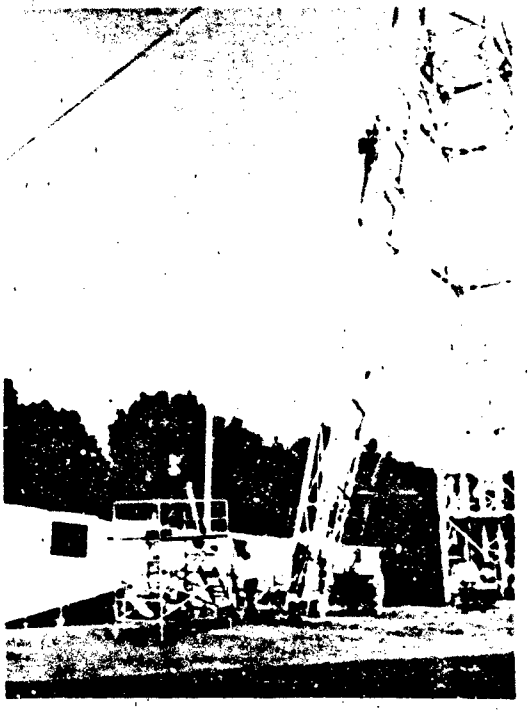

Figure 14. Test on NADC Ejection Trainer

Figure 15. Extraction of Data Using Computer System

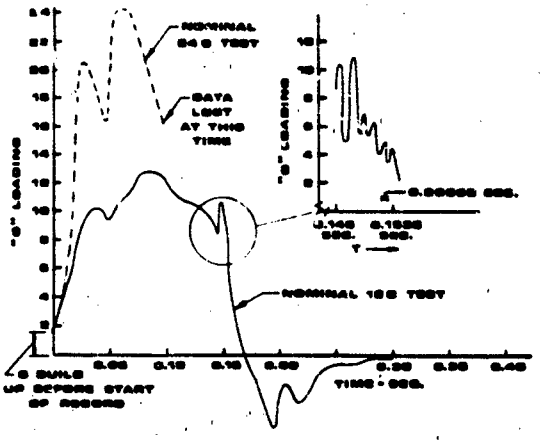

Figure 16. Acceleration Time History For NADC Tower Tests

loading. It is believed that this "dimple" in the acceleration curve is a characteristic of the pyrotechnics during its burn cycle. This peculiar behavior was confirmed by NADC as being typical for the ejection tower. It was noted on the nominal 12 G test that as the seat deceleration decreased a spike in the acceleration curve appeared just prior to a more rapid decrease in the acceleration. As shown in the expanded scale (Figure 16), a high frequency transient was encountered in the G loadings at this time. A reason for this transient oscillation (approximately 550 to 600 Hz) could not be completely resolved from discussions with the technical staff at NADC. It is believed, however, that it could have been caused by the nominal separation of part of the pyrotechnic charge from the seat. During the nominal 24 G test, all data were lost at approximately 16 Gs after the seat acceleration had decreased from the peak value of approximately 24 Gs. A real reason for the loss of the data at this point in time has not been determined. It is believed, however, that if a similar transient signal was encountered, as it was during the nominal 12 G shot, the more severe amplitude could have affected the power fail circuit of the SSMIR system or the relays in the PCM. The SSMIR system and the PCM were both checked immediately after the test shot and both were found to be operating properly.

In order to determine the cause of data loss, the SSMIR and PCM/TM system will be tested on a vibration table with sinusoidal and shock impulses throughout the pertinent frequency range with the system operating. It is believed that these tests will indicate the cause of the data drop-out so that corrective action can be undertaken to either the PCM or the SSMIR system. At the conclusion of this corrective action, it is anticipated that the SSMIR system will be demonstrated during a seat ejection test on a high speed sled track.

CONCLUDING REMARKS. It is believed that the development, test, and evaluation program reported herein has shown that a nonvolatile on-board recording and memory system has been developed which produces a viable alternative or back up to the telemetering system currently used in seat ejection testing. Since the system has been designed to fit all of the current manikins presently utilized in seat ejection testing, it would be immediately available as an advanced data system to provide rapid data retrieval at a modest cost and additional weight to the PCM/TM instrumentation system.

ACKNOWLEDGEMENT. The authors wish to express their appreciation to Thomas Gustin of SRL, whose design of the SSMIR electronic system initiated the development program, and to Robert Esken of SRL whose diligent efforts were responsible for firmware development, system checkout, and successful operation of the SSMIR system. Also, appreciation is extended to Louis D'Aulerio and Barry Shope, NADC DT&E Engineers, for their ejection tower test support and data analysis.

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